DATA SHEET

TDA8745
Satellite sound receiver with I²C-bus control

Preliminary specification
Supersedes data of 1995 Mar 08
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Philips Semiconductors

PHILIPS

Satellite sound receiver with I²C-bus control TDA8745

FEATURES

- On-chip frequency synthesizer and mixer:
  - tuning range 4 to 9.77 MHz
  - reference oscillator 4 MHz (using a crystal or 4 MHz frequency source)
- IF input switches allowing selection of various IF bandwidths (wide or narrow)
- Demodulation of two audio signals by wide band Phase-Locked Loops (PLLs)
- Audio level control after PLL (modulation depth setting)
- Noise Reduction (NR) bypass for use with main audio signals
- Left, right and mono output [½(l + r)] on SCART level
- External audio inputs (for decoder connection)
- Selectable de-emphasis (DEEM) 50 μs, 75 μs, J17 and flat response
- I²C-bus control of all functions
- Two selectable addresses
- Carrier presence detector with automatic mute option.

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8745 is the successor of the TDA8740 and TDA8741. The device contains the functionality of the TDA8740 and TDA8741 together with a synthesizer, mixer and I²C-bus control.

The pin numbers mentioned in this publication refer to the SDIP42 package; unless otherwise indicated.

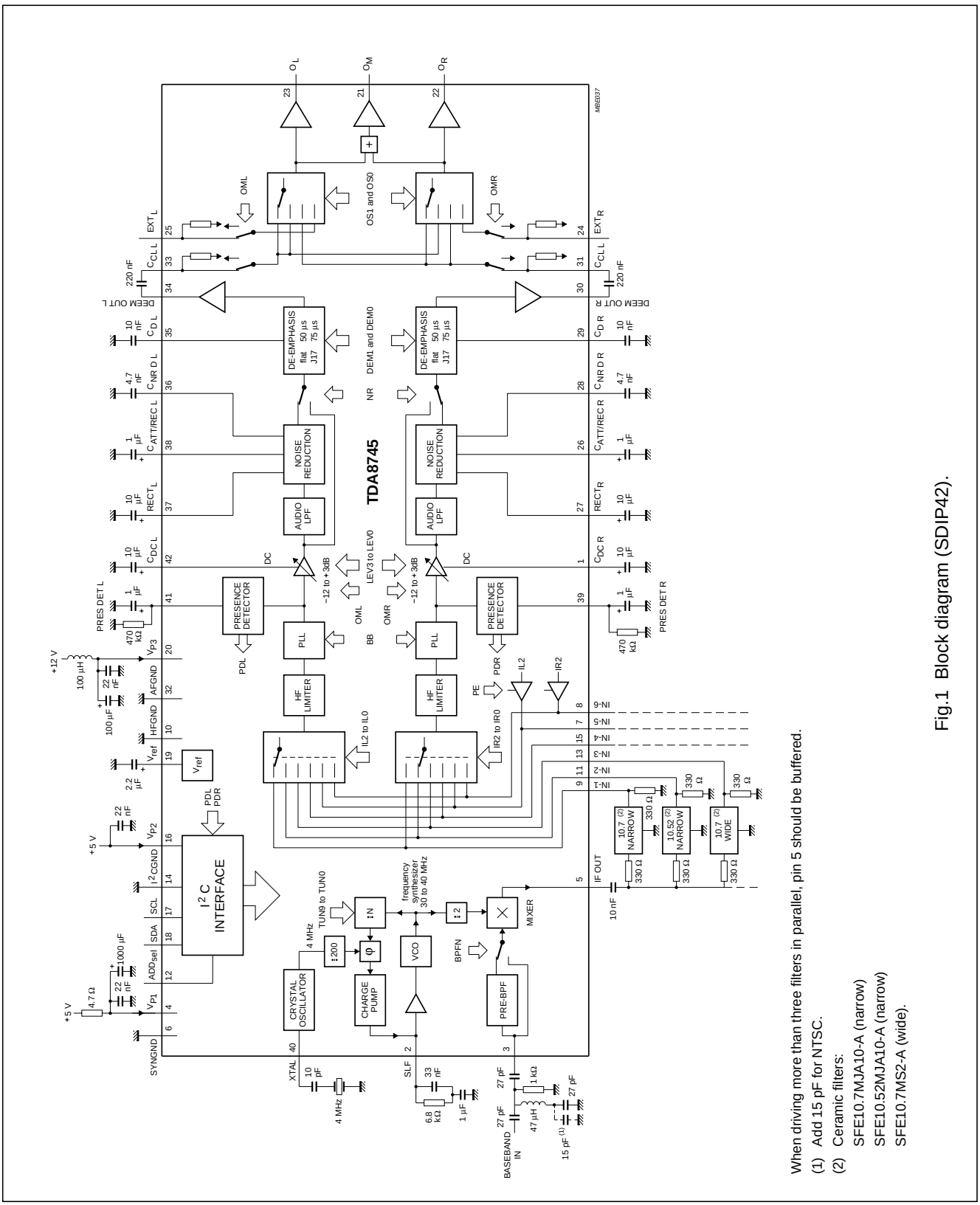
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8745	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8745H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	synthesizer and mixer supply voltage		4.5	5.0	5.5	V
V_{P2}	I²C-bus supply voltage		4.5	5.0	5.5	V
V_{P3}	general supply voltage		8.0	12.0	13.2	V
I_{P1}	synthesizer and mixer supply current		–	37	48	mA
I_{P2}	I²C-bus supply current		–	0.6	–	mA
I_{P3}	general supply current		–	35	46	mA
S/N(A)	signal-to-noise ratio secondary channel	A-weighted; NR = on; DEEM = 75 µs	68	77	–	dB
$V_{i(rms)}$	input sensitivity (RMS value) baseband input to mixer	S/N(A) = 40 dB; NR = on; DEEM = 75 µs	–	0.5	1.5	mV
$V_{i(rms)}$	baseband input voltage (RMS value)	THD ≤ 0.5%			200	mV
V_o	output voltage		–8	–6	–4	dBV
P_{tot}	total power dissipation		–	610	800	mW
T_{stg}	storage temperature		–65	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+70	°C

BLOCK DIAGRAM



When driving more than three filters in parallel, pin 5 should be buffered.

(1) Add 15 pF for NTSC.

(2) Ceramic filters:
SFE10.7MJA10-A (narrow)
SFE10.52MJA10-A (narrow)
SFE10.7MS2-A (wide).

Fig.1 Block diagram (SDIP42).

PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
$C_{DC\ R}$	1	39	DC decoupling capacitor (right channel)
SLF	2	41	synthesizer loop-filter
BASEBAND IN	3	42	baseband input to mixer
V_{P1}	4	43	synthesizer and mixer supply voltage (+5 V)
IF OUT	5	44	intercarrier output from mixer
SYNGND	6	1	synthesizer and mixer ground
IN-5	7	2	intercarrier input 5/port expansion output 1
IN-6	8	3	intercarrier input 6/port expansion output 2
IN-1	9	4	Intercarrier input 1
HFGND	10	5	HF ground
IN-2	11	6	intercarrier input 2
ADD_{sel}	12	7	I²C-bus address selection
IN-3	13	8	Intercarrier input 3
I²CGND	14	9	I²C-bus ground
IN-4	15	10	intercarrier input 4
V_{P2}	16	11	I²C-bus supply voltage (+5 V)
SCL	17	12	I²C-bus serial clock input
SDA	18	13	I²C-bus serial data input/output
V_{ref}	19	14	decoupling capacitor for reference voltage
V_{P3}	20	15	general supply voltage (+12 V)
O_M	21	17	mono channel output [½(l + r)]
O_R	22	18	right channel output
O_L	23	19	left channel output
EXT_R	24	20	external audio input (right channel)
EXT_L	25	21	external audio input (left channel)
$C_{ATT/REC\ R}$	26	22	attack/recovery capacitor (right channel)
$RECT_R$	27	23	rectifier DC decoupling (right channel)
$C_{NR\ D\ R}$	28	24	noise reduction de-emphasis capacitor (right channel)
$C_{D\ R}$	29	25	de-emphasis capacitor (right channel)
DEEM OUT R	30	26	de-emphasis output (right channel)
$C_{CL\ R}$	31	27	audio pass-through input (right channel)
AFGND	32	28	AF ground
$C_{CL\ L}$	33	29	audio pass-through input (left channel)
DEEM OUT L	34	30	de-emphasis output (left channel)
$C_{D\ L}$	35	31	de-emphasis capacitor (left channel)
$C_{NR\ D\ L}$	36	32	noise reduction de-emphasis capacitor (left channel)
$RECT_L$	37	33	rectifier DC decoupling (left channel)
$C_{ATT/REC\ L}$	38	34	attack/recovery capacitor (left channel)

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
PRES DET R	39	35	presence detector timing (right channel)
XTAL	40	36	crystal input for 4 MHz oscillator
PRES DET L	41	37	presence detector timing (left channel)
$C_{DC\ L}$	42	38	DC decoupling capacitor (left channel)
n.c.	–	16	not connected
n.c.	–	40	not connected

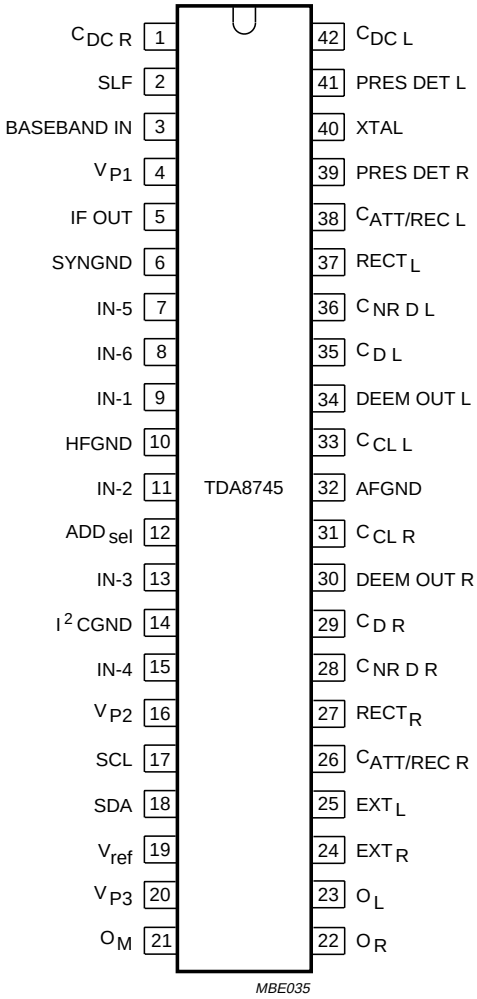


Fig.2 Pin configuration (SDIP42).

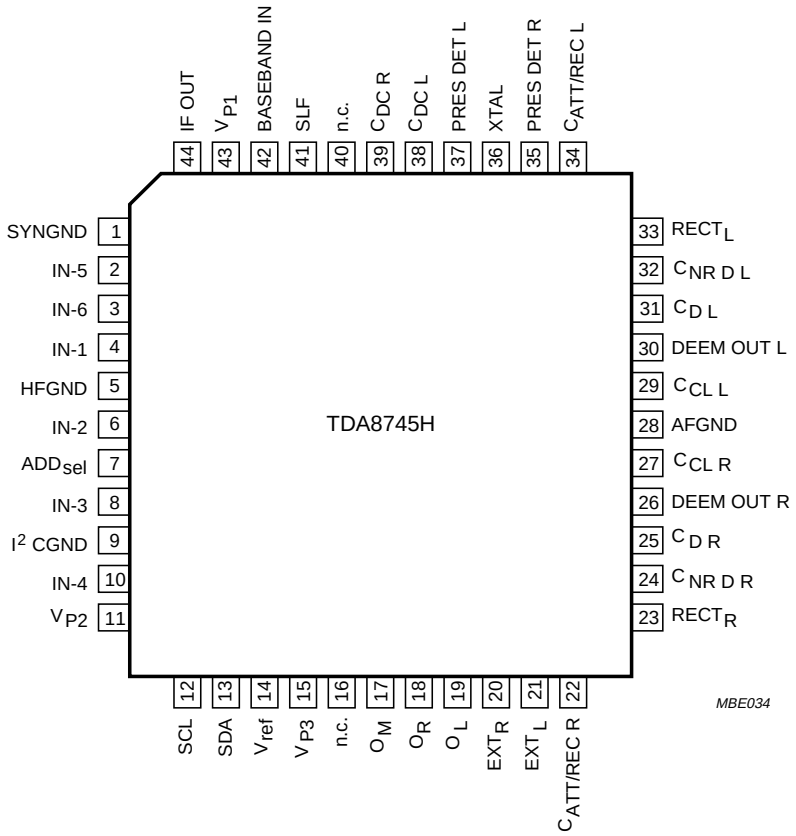


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner comprises the demodulated video signal plus a number of sound carriers in the event of reception of a PAL, NTSC or SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the mono sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present. These can be used for stereo or multi-language sound related to the video signal, or for unrelated radio sound. These carriers are also FM modulated, and for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis). These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz.

For accurate tuning to the many sound carriers, an internal frequency synthesizer and mixer are used to transfer the sound carriers to intermediate frequencies of 10.7 and 10.52 MHz.

The TDA8745 contains all circuitry for the processing of the main channel and secondary channels, from baseband signal to line (SCART) output drivers. By means of external band-pass filters the desired frequencies coming from the synthesizer/mixer are routed to the IF limiter/demodulator inputs.

Band-pass filter and mixer

Before the incoming baseband signal is applied to the mixer, the signal is filtered. Related to the sound carriers, the level of the video part of the baseband signal can be much higher, so to avoid overload it is desirable to attenuate the latter, this is also to avoid interference (additional unwanted mix of signals after mixing).

The internal band-pass filter (pass band from approximately 4 to 10 MHz) is completed by a simple external notch filter. The external filter provides substantial attenuation of the video colour carrier. The notch filter is chosen to be external because the required notch frequency is TV standard dependent and also because an accurate on-chip notch filter requires a tuning mechanism (consuming additional chip area).

The mixer is a double-balanced mixer with degeneration, this to accommodate the level of the filter output signal.

The mixer transfers the different sound carrier frequencies to fixed intermediate frequencies of 10.7 and 10.52 MHz. These frequencies are fed via an internal buffer stage to external ceramic band-pass filters before they are routed to the two demodulator inputs. The buffer stage can drive up to three external ceramic band-pass filters (assuming 330 Ω filter terminations) but this can be increased to four or more by adding an external buffer.

Synthesizer

The synthesizer consists of the following parts:

- Reference oscillator
- Reference divider
- A 10-bit programmable divider
- Phase detector
- Charge pump
- Voltage Controlled Oscillator (VCO)
- Divide-by-two circuit.

The reference frequency circuit consists of a 4 MHz crystal oscillator and a divider (by 200). The resulting reference frequency of 20 kHz is fed to the phase detector.
The programmable divider consists of a series of cells (divide by 2 or 3) connected as a ripple counter.
The minimum division ratio is 2^n and the maximum division ratio is $2^{n+1} - 1$.

The programmable divider output signal is also fed to the phase detector. The charge pump provides output current pulses in accordance with the signals from the phase detector. The final tuning voltage for the VCO is provided by the loop filter and a buffer amplifier.

The oscillator frequency range is from 29.04 to 40.94 MHz, depending on the setting of the programmable divider (by the TUN signal). The tuning voltage is clipped to limit the VCO frequency range.
The frequency of the oscillator is divided-by-two before it is applied to the mixer (to obtain the desired 10 kHz resolution).

Left and right channel inputs

A maximum of six inputs are available (pins 9, 11, 13, 15, 7 and 8). External ceramic band-pass filters, which are tuned to the desired intermediate frequencies, route the signals to the inputs.

For stereo purposes the TDA8745 contains two identical secondary sound processing channels (secondary channel 1 will also be referred to as 'left' or 'language 1' and secondary channel 2 as 'right' or 'language 2').

With the input selection every input pin of the left and/or right channel can be independently selected. Input selection for the left channel is controlled by the IL signal and for the right channel by the IR signal.

From the inputs, the signals are coupled to the limiter/amplifier and to the PLL demodulator of each channel. The output signal from the PLL is routed to both the presence detector and audio level control.

The inputs of pins 7 and 8 can be changed into digital outputs for external switching purposes, set by the so called Port Extension bit (PE). Not used inputs should be connected to ground. Note that the inputs of pins 7 and 8 are also floating when not in Port Extension mode.

Presence detector

The presence detector is used to determine if a carrier is present on the channel of interest. It does so by measuring the amount of high frequency noise (>20 kHz) in the audio signal, which is directly related to the C/N (carrier-to-noise ratio) at the IF input. If a carrier is present, these high frequencies are fairly moderate, if no carrier is present, strong noise components are present.

The audio signal, first high-pass filtered and then rectified, is filtered by the components at pins 41 and 39 (PRES DET L and PRES DET R). The DC level at this pin is then compared with an internal reference voltage. If the level at pins 41 and 39 exceeds this voltage level, the presence detector output goes HIGH (no carrier).

This output signal can be used to drive the output mute (if bit PDM = 1; see Section “Output selection”) and can be monitored by reading bits PDL and PDR. The detection level can be modified by changing the leakage resistor at pins 41 and 39, a higher resistor value gives a ‘no carrier’ response ant C/N levels detected as ‘carrier present’ with a lower resistor value.

Audio level control

Each demodulator output signal is amplified in a buffer amplifier and DC decoupled by means of electrolytic capacitors connected to pin 42 (left) and pin 1 (right).

The output level of all channels is −6 dBV typical at a frequency deviation of the FM signal of 54% of the maximum deviation (i.e 0.54×85 kHz = 46 kHz for the main channel and 0.54×50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

To adjust for different (main channel) modulation depths used at some satellites the audio level is made adjustable, the signal can be controlled in steps of 1 dB from −12 dB to +3 dB by the LEV signal.

Noise Reduction (NR)

To improve the quality of the secondary channels, the audio signal is processed at the transmitter side before modulation. For an overall flat audio response the inverse processing must take place after demodulation. This is achieved in the NR.

The NR can be regarded as an input level dependent Low-Pass Filter (LPF) [adaptive de-emphasis system] followed by a fixed de-emphasis. Figure 3 shows the transfer characteristics as function of the input level (normalized to input level, and without the fixed de-emphasis).

At maximum input level (50 kHz frequency deviation, referred to as 0 dB) the frequency response of the first part (i.e. without fixed de-emphasis) is nearly flat (note the small dip around 3 kHz in Fig.3; this is a system attribute). As the input level is X dB lowered, the higher output frequencies will be reduced an extra X dB with respect to the lower frequencies (1 : 2 expansion).

If a main carrier signal is received, the NR can be bypassed at which the signal is fed directly to the de-emphasis circuit. The noise reduction is active when the NR signal (via I²C-bus) is logic 1.

De-emphasis

De-emphasis is realized by means of several internal resistors and an external capacitor to ground. Via the I²C-bus, the DEM signal can be switched between 50 μs, 75 μs, J17 and no de-emphasis. Figure 4 shows these four different possibilities.

Output selection

With the output selector the output pins 23 and 22 can be switched to the left and right satellite channels (pins 33 and 31) or to the external inputs (pins 25 and 24) for an other signal source or for connection of a decoder box. the OS1 and OS0 bits determine this selection.

Pin 21 is a separate output which delivers the mono channel. The mono signal is the sum of pin 23 (left) and pin 22 (right) output signal [½(l + r)].

Output pins 23 and 22 can be muted by setting the OML and OMR signals to logic 1. In addition, automatic muting is also possible, the presence detector (as described in Section “Presence detector”) sets the PDL bit (PDR for other channel). Absence of a carrier at the selected frequency results in automatic muting. This mechanism is enabled or inhibited by the PDM bit (Presence Detector auto Mute).

All outputs (pins 21, 22 and 23) are line drivers with SCART level capability and are short-circuit protected by means of 125 Ω output resistors. Pins 34 and 30 are also line drivers at SCART level and can be used as signal outputs before the IC’s output selection (i.e. for decoder box use).

ABBREVIATIONS

BPF = Band-Pass Filter.

f_{mod} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

IF = Intermediate Frequency.

IL = Input Left.

IR = Input Right.

LPF = Low-Pass Filter.

NR = Noise Reduction.

OML = Output Mute Left.

OMR = Output Mute Right.

OS = Output Select.

PDM = Presence Detector auto Mute.

PE = Port Extension.

PLL = Phase-Locked Loop.

POR = Power-On Reset.

S/N = Signal-to-Noise ratio.

VCO = Voltage Controlled Oscillator.

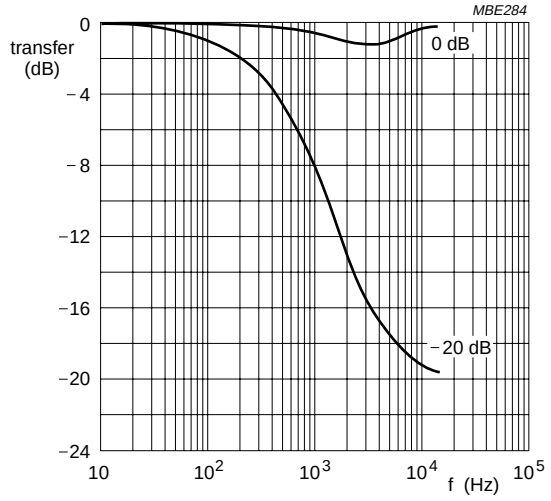


Fig.4 Noise reduction transfer as function of input level.

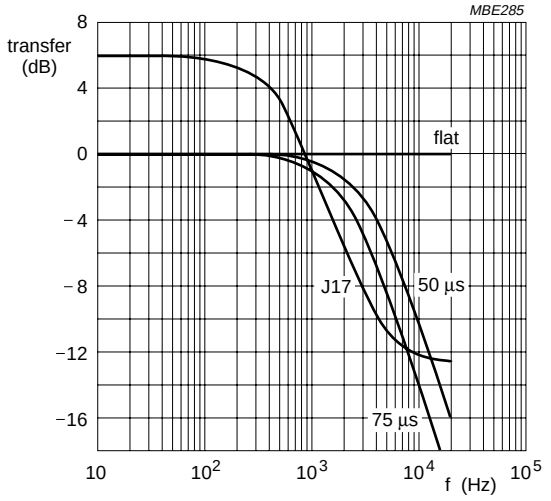


Fig.5 LF de-emphasis curves.

I²C-BUS PROTOCOL

Table 1 Slave receiver/transmitter address: D4 or D6 (HEX)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	0	1	0	1	AS(1)	R/$\overline{W}$(2)

Notes

1. AS bit defined by level at address select (pin 12); 0 V = logic 0; 5 V = logic 1.
2. R/$\overline{W}$ = 0; TDA8745 is receiver (microcontroller is master transmitter).
   R/$\overline{W}$ = 1; TDA8745 is transmitter (microcontroller is master receiver).

TDA8745 receiver use

In the receiver mode the device has four subaddresses with auto-increment, as shown in Tables 2 to 5.

Table 2 Input byte SA: 00; situation after POR

IL2 i7	IL1 i6	IL0 i5	IR2 i4	IR1 i3	IR0 i2	TUN9 i1	TUN8 i0
0	0	0	0	0	1	1	0

Table 3 Tuning byte SA: 01; situation after POR

TUN7 t7	TUN6 t6	TUN5 t5	TUN4 t4	TUN3 t3	TUN2 t2	TUN1 t1	TUN0 t0
1	1	1	0	1	1	0	0

Table 4 Select byte SA: 02; situation after POR

TEST s7	BB s6	OS1 s5	OS0 s4	PDM s3	PE s2	OML s1	OMR s0
0	0	0	0	0	0	1	1

Table 5 Audio byte SA: 03; situation after POR

LEV3 a7	LEV2 a6	LEV1 a5	LEV0 a4	NR a3	DEM1 a2	DEM0 a1	BPFN a0
1	1	0	0	1	1	1	0

TDA8745 transmitter use

No subaddress.

Table 6 Read byte

PDL r7	PDR r6	– r5	– r4	– r3	– r2	– r1	POR r0
0 or 1	0 or 1	1	1	1	1	1	0 or 1

Slave receiver mode (bits transmitted from microcontroller to TDA8745)

Different IF inputs can be selected for the PLLs, for switching between different external BPFs and/or channels; see Tables 7 and 8.

Table 7 IL2 to IL0; Input Left; note 1

IL2 i7	IL1 i6	IL0 i5	PE(2) s2	MODE
0	0	0	0	IF input IN-1 selected for left PLL (after POR)
0	0	1	0	IF input IN-2 selected for left PLL
0	1	0	0	IF input IN-3 selected for left PLL
0	1	1	0	IF input IN-4 selected for left PLL
1	0	0	0	IF input IN-5 selected for left PLL
1	0	1	0	IF input IN-6 selected for left PLL
1	1	0	0	no selection
1	1	1	0	no selection
X	0	0	1	IF input IN-1 selected for left PLL
X	0	1	1	IF input IN-2 selected for left PLL
X	1	0	1	IF input IN-3 selected for left PLL
X	1	1	1	IF input IN-4 selected for left PLL
0	X	X	1	IF input IN-5 used as output; 0 = 0 V
1	X	X	1	IF input IN-5 used as output; 1 = 5 V

Notes

1. X = don’t care.
2. Bit PE (s2) can be set to logic 1 to change IF input 5 into digital output for external switching purposes.

Table 8 IR2 to IR0; input right; note 1

IR2 i4	IR1 i3	IR0 i2	PE[2] s2	MODE
0	0	0	0	IF input IN-1 selected for right PLL
0	0	1	0	IF input IN-2 selected for right PLL (after POR)
0	1	0	0	IF input IN-3 selected for right PLL.
0	1	1	0	IF input IN-4 selected for right PLL
1	0	0	0	IF input IN-5 selected for right PLL
1	0	1	0	IF input IN-6 selected for right PLL
1	1	0	0	no selection
1	1	1	0	no selection
X	0	0	1	IF input IN-1 selected for right PLL
X	0	1	1	IF input IN-2 selected for right PLL
X	1	0	1	IF input IN-3 selected for right PLL
X	1	1	1	IF input IN-4 selected for right PLL
0	X	X	1	IF input IN-6 used as output; 0 = 0 V
1	X	X	1	IF input IN-6 used as output; 1 = 5 V

Notes

1. X = don’t care.
2. Bit PE (s2) can be set to logic 1 to change IF input 6 into digital output for external switching purposes.

Table 9 TUN9 to TUN0; tuning

TUN9 i1	TUN8 i0	TUN7 t7	TUN6 t6	TUN5 t5	TUN4 t4	TUN3 t3	TUN2 t2	TUN1 t1	TUN0 t0	10.7 IF (MHz)	10.52 IF (MHz)
0	1	1	0	1	0	1	1	0	0	3.82	4.00
0	1	1	0	1	0	1	1	0	1	3.83	4.01
0	1	1	0	1	0	1	1	1	0	3.84	4.02
0110101111 to 1001010011										3.85 to 5.49	4.03 to 5.67
1	0	0	1	0	1	0	1	0	0	5.50	5.68
1001010101 to 1010000101										5.51 to 5.99	5.69 to 6.17
1	0	1	0	0	0	0	1	1	0	6.00	6.18
1010000111 to 1010110111										6.01 to 6.49	6.19 to 6.67
1	0	1	0	1	1	1	0	0	0	6.50	6.68
1010111001 to 1011101011										6.51 to 7.01	6.69 to 7.19
1	0	1	1	1	0	1	1	0	0	7.02(1)	7.20(1)
1011101101 to 1100001111										7.03 to 7.37	7.21 to 7.55
1	1	0	0	0	1	0	0	0	0	7.38	7.56
1100010001 to 1100110011										7.39 to 7.73	7.57 to 7.91
1	1	0	0	1	1	0	1	0	0	7.74	7.92
1100110101 to 1111111100										7.75 to 9.74	7.93 to 9.92
1	1	1	1	1	1	1	1	0	1	9.75	9.93
1	1	1	1	1	1	1	1	1	0	9.76	9.94
1	1	1	1	1	1	1	1	1	1	9.77	9.95

Note

1. This is the situation after POR.

The frequency range of synthesizer is shown in Table 10.

Table 10 Frequency range of synthesizer

PARAMETER	RANGE (MHz)
Synthesizer frequency range	29.04 to 40.94 (in 20 kHz grid); note 1
Mixer input frequency range	14.52 to 20.47 (in 10 kHz grid); note 2
Tuning range	3.82 to 9.77 (in 10 kHz grid; 10.7 MHz IF); note 3

Notes

1. Tuning the synthesizer below 29.04 MHz may be possible, but is not guaranteed.
2. The mixing frequency (f_{mix}) can be calculated with equation:
   f_{mix} = (1024 + 512[TUN9] + 256[TUN8] + 128[TUN7] + 64[TUN6] + 32[TUN5] + 16[TUN4] + 8[TUN3] + 4[TUN2] + 2[TUN1] + [TUN0]) × 10 kHz.
3. Tuning frequency = mixer input frequency – 10.7 MHz.

Table 11 Bit TEST

TEST s7	MODE	DESCRIPTION
0	– (POR)	in applications this bit should always be logic 0, to avoid conflicts with other settings
1	test	setting TEST enables some special modes used for factory testing

Table 12 Bit BB; baseband; note 1

BB s6	MODE	DESCRIPTION
0	synthesizer	synthesizer use (PLLs central frequency approximately 10.7 MHz) (after POR)
1	baseband	baseband use (PLLs central frequency approximately 6 MHz)

Note

1. The PLL demodulators can also be used for demodulating FM carriers (e.g. terrestrial TV sound) at baseband frequencies, by changing the lock range of the PLLs.

Table 13 Bits OS1 and OS0; output select; note 1

OS1 s5	OS0 s4	MODE	DESCRIPTION
0	0	stereo (POR)	Left channel audio (pin 33) at O_L; right channel audio (pin 31) at O_R
0	1	left	Left channel audio (pin 33) at both O_L and O_R
1	0	right	Right channel audio (pin 31) at both O_L and O_R
1	1	external	External left at (pin 25) at O_L; external right (pin 24) at O_R

Note

1. The signal at both line outputs O_L and O_R (pins 23 and 22) can be selected with bits OS1 and OS0.

Table 14 Bit PDM; Presence Detector auto Mute; note 1

PDM s3	MODE	DESCRIPTION
0	– (POR)	–
1	PDM	if this bit is set to logic 1, a channel for which no incoming carrier is found will be muted

Note

1. In both situations the status of the presence detector can be monitored by reading the bits PDL (r7) and PDR (r6) back from the IC. Appropriate action (e.g. muting, channel selection or tuning) can then be taken by the microcontroller. Note that this function also mutes the signal from the external inputs (pins 25 and 24). This may be desirable when using these inputs for connecting a satellite descrambler box. If not, reset PDM (s3) to logic 0 when selecting external [e.g. together with bits OS1 (s5) and OS0 (s4)].

Table 15 Bit PE; Port Extension; note 1

PE s2	DESCRIPTION
0	6 IF inputs; no digital output (after POR)
1	4 IF inputs; 2 digital outputs

Note

1. Two IF inputs (IN-5 and IN-6; pins 7 and 8) can be used as digital output instead. If no more than four IF inputs are needed, two external functions can be controlled via the I²C-bus this way. The level at these pins is controlled by bits IL2 (i7) and IR2 (i4); see Tables 7 and 8.

Table 16 Bits OML and OMR; Output Mute Left and Output Mute Right; note 1

BIT	LEVEL	MODE	DESCRIPTION
OML (s1)	0	–	–
	1	mute	Left audio channel is muted
OMR (s0)	0	–	–
	1	mute	Right audio channel is muted

Note

1. Left and right audio can be muted independently. Note that also the external input signals (pins 25 and 24) can be muted this way.

Table 17 Bits LEV3 to LEV0; level adjust; note 1

LEV3 a7	LEV2 a6	LEV1 a5	LEV0 a4	MODE	SECONDARY CHANNELS(2) (kHz)	MAIN CHANNEL(2) (kHz)
0	0	0	0	–12 dB	199	338
0	0	0	1	–11 dB	177	302
0	0	1	0	–10 dB	158	269
0	0	1	1	–9 dB	141	240
0	1	0	0	–8 dB	126	214
0	1	0	1	–7 dB	112	190
0	1	1	0	–6 dB	100	170
0	1	1	1	–5 dB	89	151
1	0	0	0	–4 dB	79	135
1	0	0	1	–3 dB	71	120
1	0	1	0	–2 dB	63	107
1	0	1	1	–1 dB	56	95
1	1	0	0	0 dB	50(3)	85(3)
1	1	0	1	+1 dB	45	76
1	1	1	0	+2 dB	40	68
1	1	1	1	+3 dB	35	60

Notes

1. The audio level can be adjusted in steps of 1 dB, to adjust for different FM deviations used in main channel audio carriers and/or spread in PLL output amplitude. With secondary carriers the Noise Reduction (NR) is to be used with the 0 dB setting (note that the NR audio frequency response is level dependent, therefore another setting than 0 dB is only to be used when making a fine-adjustment (+2 dB/–2 dB) for PLL spread. Typical setting for main channel carriers is in most cases 85 kHz (0 dB) or 76 kHz (+1 dB).
2. Maximum deviation.
3. Situation after POR.

Table 18 Bit NR; Noise Reduction; note 1

NR a3	MODE	DESCRIPTION
0	NR bypassed	Noise Reduction bypassed (main channel)
1	NR active	Noise Reduction active (secondary channels) (after POR)

Note

1. For reception of main channel carriers the NR circuit can be bypassed.

Table 19 Bits DEM1 and DEM0; De-emphasis; note 1; see Fig.5

DEM1 a2	DEM0 a1	DE-EMPHASIS
0	0	no de-emphasis (flat)
0	1	J17
1	0	50 μs(2)
1	1	75 μs [por](3)

Notes

1. Different de-emphasis characteristics can be selected, to adjust for different main channel audio carriers.
2. In most cases the de-emphasis needed for main channel carriers is 50 μs.
3. The NR is to be used with the 75 μs setting for standard secondary channels.

Table 20 Bit BPFN; Band-Pass Filter Not; note 1

BPFN a0	DESCRIPTION
0	mixer input signal filtered by BPF (after POR)
1	mixer input signal is not filtered

Note

1. To avoid interference by the video signal, the incoming baseband signal is filtered. If this filtering is not required the filter can be switched off.

Slave transmitter mode (bits transmitted from TDA8745 to microcontroller)

Table 21 Bit PDL; Presence Detector Left; note 1

PDL r7	DESCRIPTION
0	carrier detected at left channel
1	no carrier detected at left channel

Note

1. Bit PDL (r7) transmits the current status of the left channel presence detector. When PDL = 1, no carrier is found at the currently selected frequency. If bit PDM (s3) = 0 the left channel audio is muted.

Table 22 Bit PDR; Presence Detector Right; note 1

PDR r6	DESCRIPTION
0	carrier detected at right channel
1	no carrier detected at right channel

Note

1. Bit PDR (r6) transmits the current status of the right channel presence detector. When PDR = 1, no carrier is found at the currently selected frequency. If bit PDM (s3) = 0 the right channel audio is muted.

Table 23 Bit POR; Power-On Reset; note 1

POR r0	DESCRIPTION
0	normal operation
1	POR generated; power dip detected since last read of POR bit

Note

1. At switching on, or after a power dip on the I²C-bus supply voltage (V_{P2}), an internal signal is generated which resets the I²C-bus registers to a pre-defined state. If bit POR (r0) = 1, such a situation has occurred since the last time the read byte was read. After reading, the bit is reset to logic 0.

Table 24 Bits r5 to r1

– r5	– r4	– r3	– r2	– r1	DESCRIPTION
1	1	1	1	1	These bits have no function. Although their state is fixed, the microcontroller should not rely on this because of eventual future use.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	synthesizer and mixer supply voltage	note 1	0	5.5	V
V_{P2}	I²C-bus supply voltage	note 1	0	5.5	V
V_{P3}	general supply voltage	note 1	0	13.2	V
V_n	voltage on pins 2, 3, 5 and 40	note 1	0	5.5	V
	voltage on pins 7 and 8	note 2	0	V_{P2}	V
	voltage on pins 1 and 42	note 1	0	7.7	V
V_i	input voltage on pins 7, 8, 9, 11, 13 and 15	notes 1 and 3	0	1	V
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C

Notes

1. All voltages referenced to ground at pins 6, 10, 14 and 32.
2. Port Extension enabled (PE = 1; see Table 15).
3. IN-5 and IN-6 (pins 7 and 8) **not** being in the Port Extension mode.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	50	K/W
	QFP44	60	K/W

DC CHARACTERISTICS

All voltages referenced to ground (pins 6, 10, 14 and 32). In accordance with the block diagram (see Fig.1); $V_{P1} = V_{P2} = 5$ V; $V_{P3} = 12$ V; $T_{amb} = 25$ °C; $f_{OS1} = 10.7$ MHz; $f_{OS2} = 10.52$ MHz (no modulation; see note 1); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	synthesizer and mixer supply voltage		4.5	5.0	5.5	V
V_{P2}	I²C-bus supply voltage		4.5	5.0	5.5	V
V_{P3}	general supply voltage		8.0	12	13.2	V
I_{P1}	synthesizer and mixer supply current		–	37	48	mA
I_{P2}	I²C-bus supply current		–	0.6	–	mA
I_{P3}	general supply current		–	35	46	mA
P_{tot}	total power dissipation		–	610	800	mW
Pins						
$V_{21,22,23}$	voltage on pins 21, 22 and 23		–	3.8	–	V
$V_{24,25,31,33}$	voltage on pins 24, 25, 31 and 33		–	3.8	–	V
$V_{31,33}$	voltage on pins 31 and 33		–	3.8	–	V
$V_{30,34}$	voltage on pins 30 and 34		–	3.8	–	V
$V_{27,37}$	voltage on pins 27 and 37		–	3.8	–	V
V_{19}	voltage on pin 19		3.7	3.8	3.9	V
$V_{9,11,13,15}$	voltage on pins 9, 11, 13 and 15	note 2	–	0	–	V
$V_{42,1}$	voltage on pins 42 and 1		–	3.4	–	V
$V_{41,39}$	voltage on pins 41 and 39		–	2.6	–	V
V_5	voltage on pin 5		–	1.8	–	V
V_3	voltage on pin 3		–	2.4	–	V
V_2	voltage on pin 2		–	2.6	–	V
V_{40}	voltage on pin 40		–	1.3	–	V
Port extensions (pins 7 and 8; bit PE = 1)						
V_{OH}	HIGH level output voltage	$I_{OH} = 0.5$ mA	4.5	–	5	V
V_{OL}	LOW level output voltage	$I_{OL} = -0.5$ mA	0	–	0.5	V

Notes

1. Presence of both carriers is required to achieve lock of the PLLs; otherwise not all pins will have a stable DC voltage.
2. Pin 7 and 8 functioning as normal inputs (bit PE = 0).

AC CHARACTERISTICS

All voltages referenced to ground (pins 6, 10, 14 and 32); in accordance with the block diagram (see Fig.1); $V_{P1} = V_{P2} = 5$ V; $V_{P3} = 12$ V; $T_{amb} = 25$ °C; $f_{mod} = 1$ kHz; $\Delta f_M = 46$ kHz; $\Delta f_{S1} = \Delta f_{S2} = 27$ kHz (reference levels); $f_{OM} = 10.7$ MHz; $f_{OS1} = 10.7$ MHz; $f_{OS2} = 10.52$ MHz; IF level at pins 9, 11, 13, 15, 7 and 8 = 20 mV (RMS value) and SFE 10.7MJA (narrow), SFE 10.52MJA (narrow) and SFE 10.7MS3 (wide) ceramic filters; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band-pass filter, mixer and buffer						
R_i	input resistance		10	12.5	15	kΩ
$V_{i(rms)}$	baseband input voltage (RMS value)	note 1	–	–	200	mV
V_3	1 dB compression point (RMS value)	$\Delta V_3 - \Delta V_5 = 1$ dB; note 2	–	180	–	mV
H_l/H_h	filter transfer at 200 kHz with respect to 7.3 MHz		–	–	–60	dB
H_{lm}/H_h	filter transfer at 2 MHz with respect to 7.3 MHz		–	–28	–20	dB
H_{mh}/H_h	filter transfer at 5.3 MHz with respect to 7.3 MHz		–2	+2	+4	dB
H_h*A	filter transfer at 7.3 MHz and mixer amplification		15	17	19	dB
H_h*C	filter transfer at 7.3 MHz and mixer conversion gain	note 3	10	12	14	dB
$I_{o(p)}$	mixer output current (peak)		5	7	–	mA
R_o	mixer output resistance	f = 10.7 MHz; note 4	–	12	30	Ω
Charge pump, buffer amplifier and VCO						
t	repetition time of charge pump pulses		–	50	–	µs
S_{VCO}	VCO sensitivity	note 5	–	–9	–	MHz/V
f_{VCO}	VCO frequency	$V_{loopf} = 2.6$ V	–	35.4	–	MHz
Crystal oscillator (4 MHz)						
f_{xtal}	crystal oscillator frequency		–	4	–	MHz
R_{xtal}	resonance resistance of crystal		–	–	60	Ω
C_{xtal}	parallel capacitance of crystal		–	4.5	10	pF
$I_{i(p)}$	input current from external 4 MHz source (peak)	note 6	50	–	–	µA
IF inputs (pins 9, 11, 13, 15, 7 and 8) and limiters						
$V_{IN-1\ to\ IN-6(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB; $\Delta f_S = 27$ kHz; NR = on; de-emphasis = 75 µs	–	0.3	1	mV
		S/N(A) = 40 dB; $\Delta f_M = 46$ kHz; NR = off; de-emphasis = 50 µs	–	0.8	2	mV
V_{i1} to V_{i6}	input signal	THD ≤ 0.5%	–	–	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulators						
f_{CCO}	free-running frequency	PLL left; BB = 0	–	10.6	–	MHz
		PLL right; BB = 0	–	10.6	–	MHz
		PLL left; BB = 1	–	6.9	–	MHz
		PLL right; BB = 1	–	6.9	–	MHz
Δf_{CCO}	lock range of PLLs	BB = 0; note 7	10	–	11.5	MHz
		BB = 1; note 7	5.50	–	8.50	MHz
V_{OL}; V_{OR}	PLL output voltage (pins 23 and 22)	NR = off; DEEM = flat; BB = 0	–	–5.6	–	dBV
		NR = off; DEEM = flat; BB = 1; note 8	–	–7.3	–	dBV
ΔV_{OL}; ΔV_{OR}	spread of PLL output voltage over lock range (pins 23 and 22)	NR = off; DEEM = flat; BB = 1; note 8	–	–	±1.5	dB
Noise reduction						
$\frac{V_{37,27\ (50\ kHz)}}{V_{37,27\ (1\ kHz)}}$	low-pass filter 50 kHz response with respect to 1 kHz	note 9	–21	–16	–11	dB
$V_{o\ 23,22}$	output voltage (pins 23 and 22)	at 0 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; DEEM = flat; note 10	–1	+1	+3	dBV
		at –20 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; DEEM = flat	–29	–26	–23	dBV
$\frac{V_{23,22\ (15\ kHz)}}{V_{23,22\ (1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz	at 0 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; DEEM = flat	–2	0	+2	dB
		at –20 dB NR input level; $\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; DEEM = flat	–13	–11.5	–10	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors (pins 38 and 26)	$\Delta f = 0$ kHz; all PLLs locked	14	–	22	mV
De-emphasis						
$\frac{V_{23,22\ (15\ kHz)}}{V_{23,22\ (1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz flat	NR = off; DEEM = flat	–0.5	0.0	+0.5	dB
		NR = off; DEEM = J17; note 11	–13.9	–12.4	–10.9	dB
		NR = off; DEEM = 50 µs	–15.2	–13.7	–12.2	dB
		NR = off; DEEM = 75 µs	–18.6	–17.1	–15.6	dB
R_o	output resistance (pins 34 and 30)		100	125	150	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall performance						
$V_{i\ 3(rms)}$	baseband input sensitivity main sound carrier (RMS value)	S/N(A) = 40 dB; Δf_S = 27 kHz; NR = on; DEEM = 75 µs	–	0.5	1.5	mV
		S/N(A) = 40 dB; Δf_M = 46 kHz; NR = off; DEEM = 50 µs	–	1.5	3	mV
$V_{o\ 23,22}$	output voltage	secondary channels; Δf_S = 27 kHz; NR = on; DEEM = 75 µs	–8	–6	–4	dBV
		main channel; Δf_S = 46 kHz; NR = off; DEEM = 50 µs	–8	–6	–4	dBV
UBS	unbalance output voltage	secondary channels; NR = on; DEEM = 75 µs	–1	–	+1	dBV
		main channel; NR = off; DEEM = 50 µs	–1	–	+1	dBV
THD	total harmonic distortion	secondary channels; NR = on; DEEM = 75 µs; note 12	–	0.1	0.5	%
		main channel; NR = off; DEEM = 50 µs; note 12	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; secondary channels (synthesizer included); NR = on; DEEM = 75 µs; note 12	69	77	–	dB
		A-weighted; secondary channels (synthesizer excluded); NR = on; DEEM = 75 µs; note 12	72	80	–	dB
		A-weighted; main channel (synthesizer included); NR = off; DEEM = 50 µs; note 12	54	62	–	dB
		A-weighted; main channel (synthesizer excluded); NR = off; DEEM = 50 µs; note 12	62	70	–	dB
$MUTE_{att}$	mute attenuation	output select left and right muted	74	90	–	dB
$\alpha_{ct\ S/S}$	crosstalk attenuation between secondary channels		–	74	–	dB
$SVRR_{P3}$	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz; NR = on; DEEM = 75 µs	–	14.3	–	dB
		V_{RR} = 100 mV; f_i = 1 kHz; NR = on; DEEM = 75 µs	–	15.6	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$SVRR_{P1-P2}$	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz; NR = on; DEEM = 75 µs	–	25	–	dB
		V_{RR} = 100 mV; f_i = 1 kHz; NR = on; DEEM = 75 µs	–	4	–	dB
Output select						
$V_{i\ 25,24}$	input voltage (pins 25 and 24)		–	–	8	dBV
$R_{i\ 25,24,33,31}$	input resistance at pins 25, 24, 33 and 31		100	150	200	kΩ
$V_{o\ 23,22}$	output voltage at pins 23 and 22	$V_{24,25}$ = –6 dBV; OS = external	–6.5	–6	–5.5	dBV
$R_{o\ 23,22,21}$	output resistance at pins 23, 22 and 21		100	125	150	Ω
THD	total harmonic distortion	$V_{24,25}$ = –6 dBV; OS = external; f = 1 kHz	–	0.01	0.3	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{24,25}$ = –6 dBV; OS = external	80	–	–	dB
$\alpha_{ct\ L/R}$; $\alpha_{ct\ R/L}$	crosstalk between channels	f = 1 kHz	–	80	–	dB
I²C-bus						
C_i	input capacitance		–	4	–	pF
I_{sink}	SDA sink current		3	–	–	mA
V_{IH}	HIGH level input voltage		3	–	5	V
V_{IL}	LOW level input voltage		0	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
Address D4H	address D4H	ADD_{sel} = LOW	0	–	1	V
Address D6H	address D6H	ADD_{sel} = HIGH	3	–	5	V
f_{SCL}	SCL frequency		–	–	100	kHz

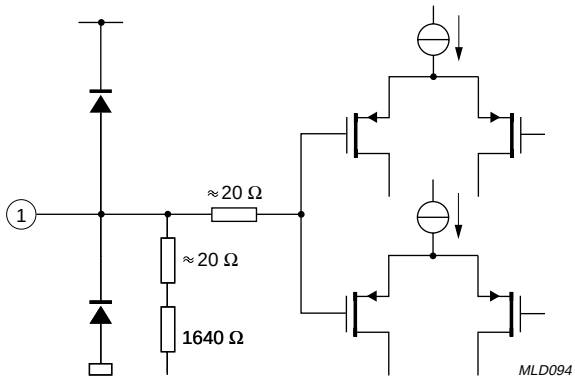
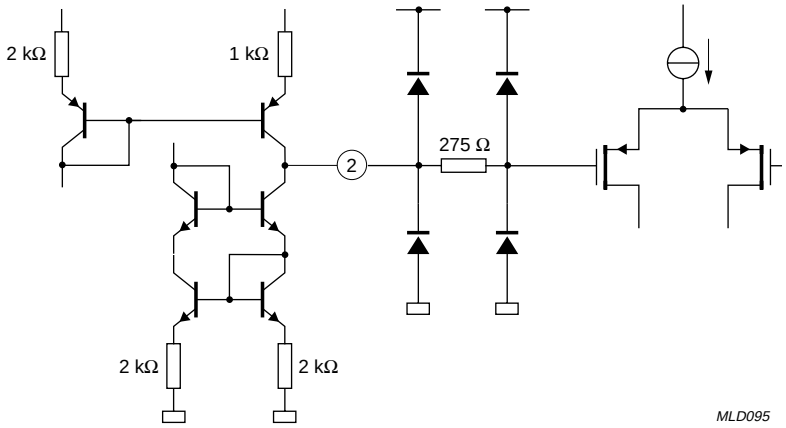
Notes

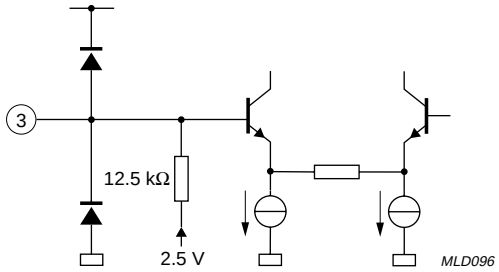
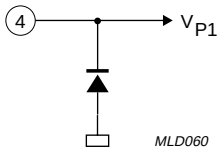
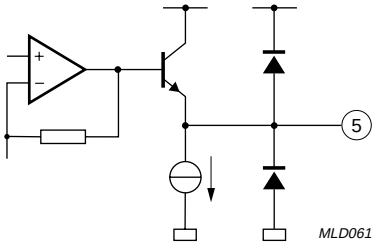
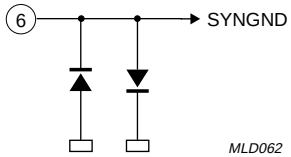
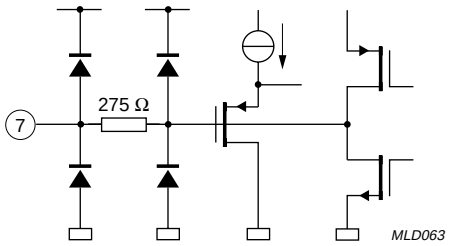
1. Maximum of 0.5% THD at LF outputs.
2. When the increase of the output signal (pin 5 at 10.7 MHz) lags 1 dB behind the increase of the input signal (pin 3; 7.02 MHz carrier), the so called 1 dB compression point is reached. For complex signals (more than one sound carrier), this point will shift to a higher value.
3. The mixer performs both a mixing and amplifying action (normal operation). The synthesizer is tuned to the 7.3 MHz incoming carrier.
4. The buffer output is sensitive to capacitive loading, therefore (capacitive) loads other than those present in the block diagram (see Fig.1) should be avoided.
5. As present at the mixer output (pin 5) in ‘BPFTILT’ test mode the actual VCO sensitivity is two times the given value because of the divide-by-two circuit between VCO output and mixer.
6. The required 4 MHz crystal can be omitted if this frequency is already available in the application. This signal source should be connected to pin 40, via a capacitor in series with a resistor R_{ext}. The minimum required AC current is 50 µA, determined by the resistors R_{int} and R_{ext} and the level of the 4 MHz AC voltage. The value of R_{int} is 700 Ω and the signal shape of the signal is not important.

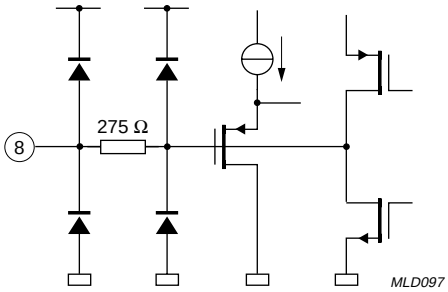
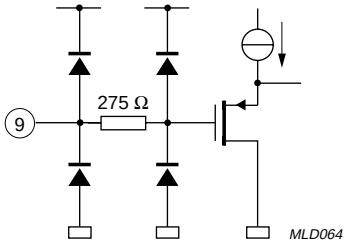
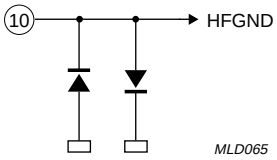
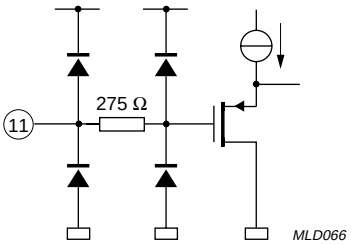
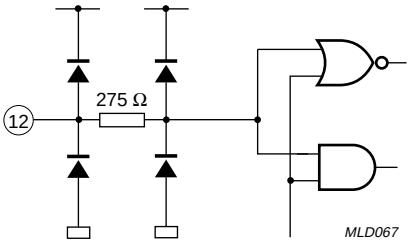
7. Maximum THD of 0.5%; 8 V < V_{P3} < 13.2 V; 0 °C < T_{amb} < 70 °C. Measured at pins 34 and 30; NR = off; DEEM = flat.
8. Correction of output voltage is possible by correcting the volume level.
9. Measured at pins 37 and 27 with no electrolytic capacitors connected to these pins.
10. Input level of 0 dB; signal level in accordance with $\Delta f_{S1} = \Delta f_{S2}$ = 50 kHz. At this input level, the NR response is equal for high and low frequencies (see Fig.4).
11. J17 de-emphasis includes +6 dB amplification (see Fig.5).
12. Both PLLs locked.

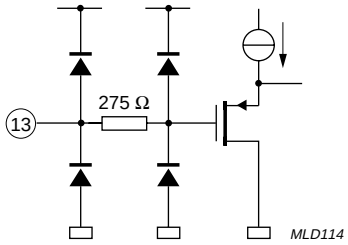
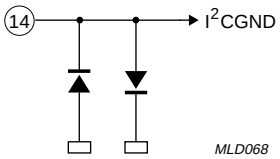
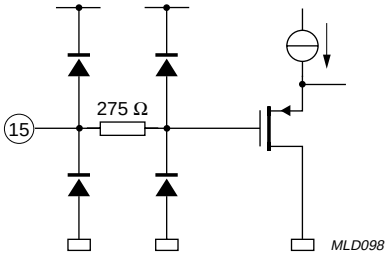
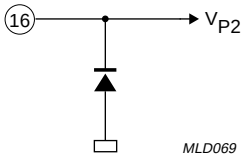
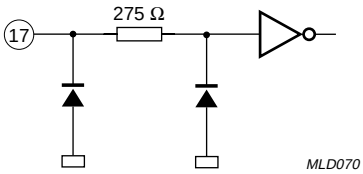
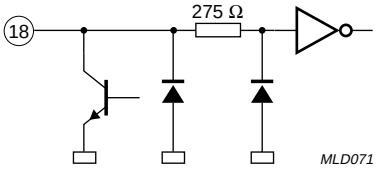
INTERNAL CIRCUITRY

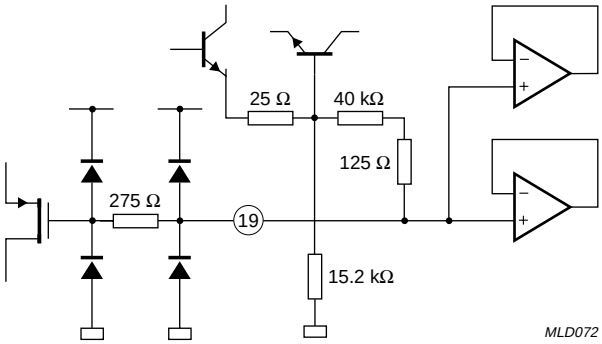
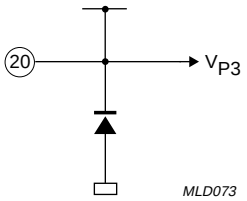
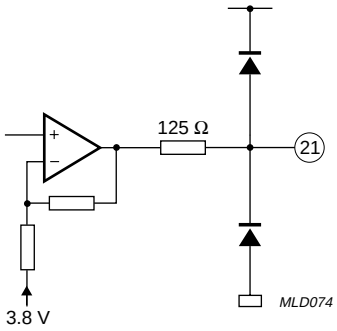
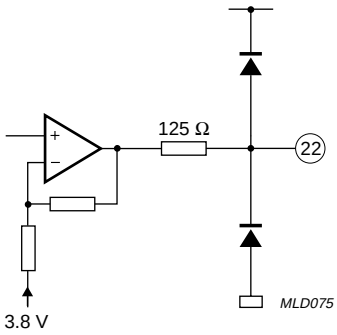
For description see Chapter “Pinning”.

SYMBOL	PIN	EQUIVALENT CIRCUIT
$C_{DC\ R}$	1	
SLF	2	

SYMBOL	PIN	EQUIVALENT CIRCUIT
BASEBAND IN	3	
V_{P1}	4	
IF OUT	5	
SYNGND	6	
IN-5	7	

SYMBOL	PIN	EQUIVALENT CIRCUIT
IN-6	8	
IN-1	9	
HFGND	10	
IN-2	11	
ADD_{sel}	12	

SYMBOL	PIN	EQUIVALENT CIRCUIT
IN-3	13	
I²CGND	14	
IN-4	15	
V_{P2}	16	
SCL	17	
SDA	18	

SYMBOL	PIN	EQUIVALENT CIRCUIT
V_{ref}	19	
V_{P3}	20	
O_M	21	
O_R	22	

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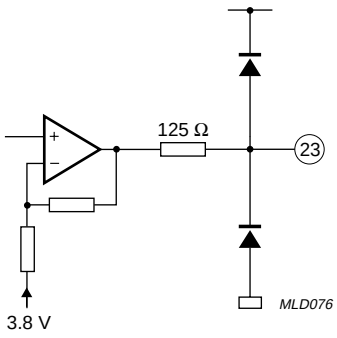
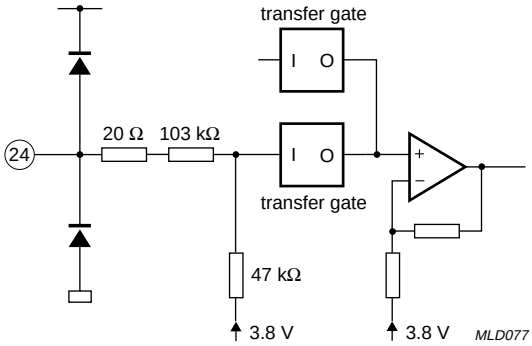
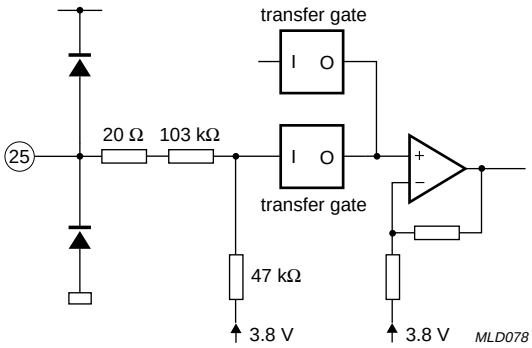
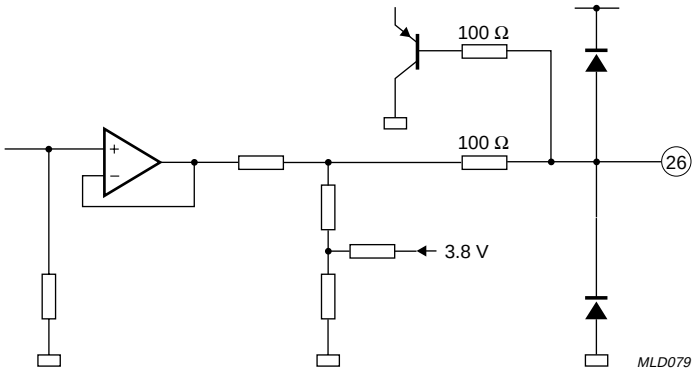
O_L	23	
EXT_R	24	
EXT_L	25	
$C_{ATT/REC\ R}$	26	

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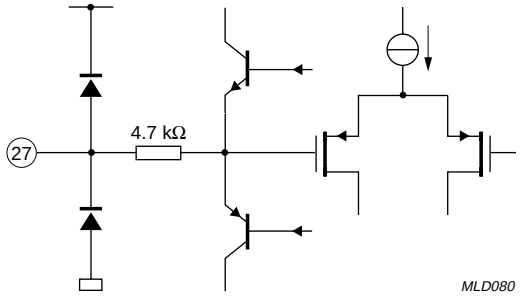
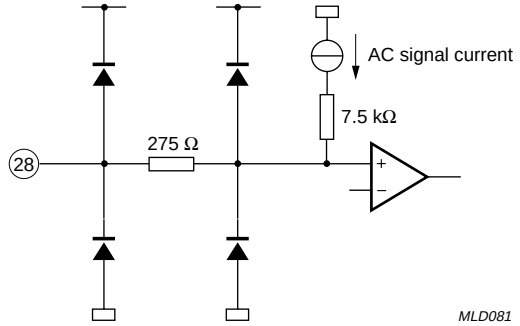
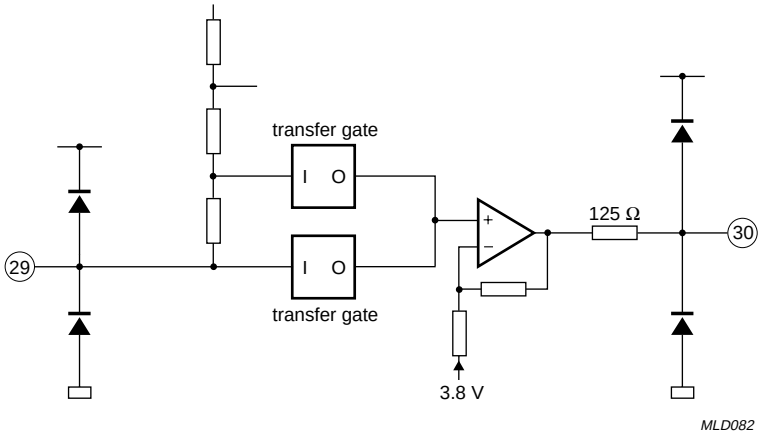
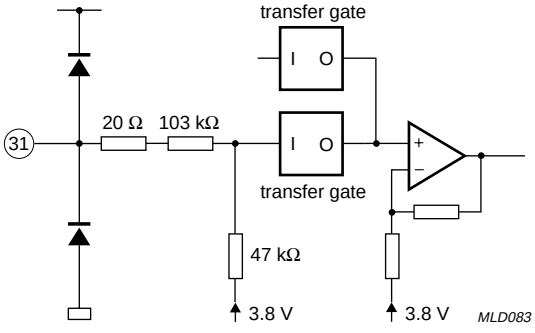
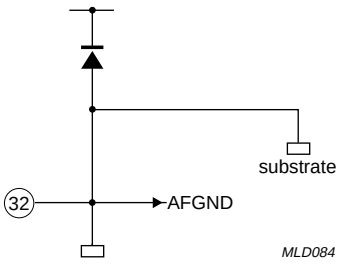
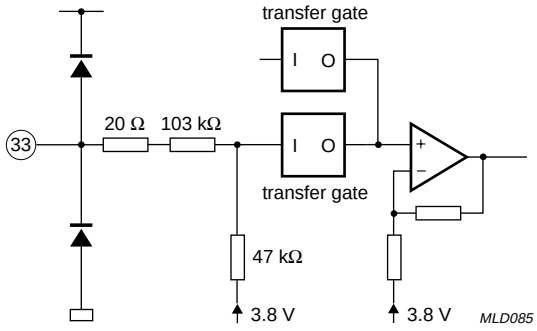
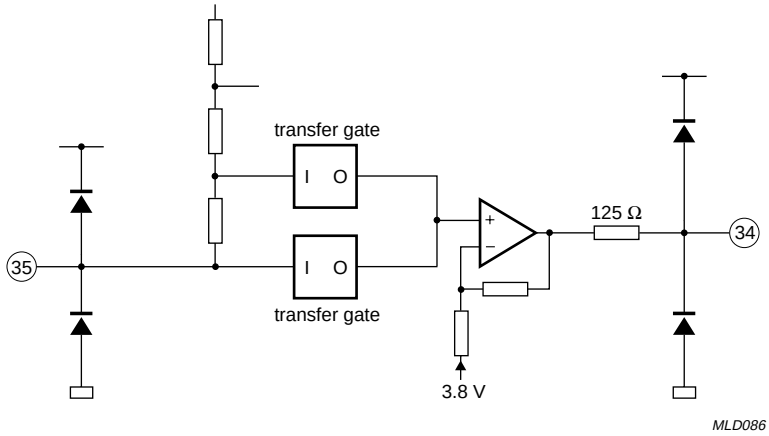
$RECT_R$	27	
$C_{NR\ D\ R}$	28	
$C_{D\ R}$	29	
DEEM OUT R	30	
$C_{CL\ R}$	31	

SYMBOL	PIN	EQUIVALENT CIRCUIT
AFGND	32	
$C_{CL\ L}$	33	
DEEM OUT L	34	
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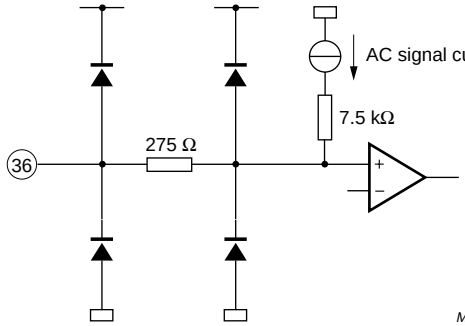
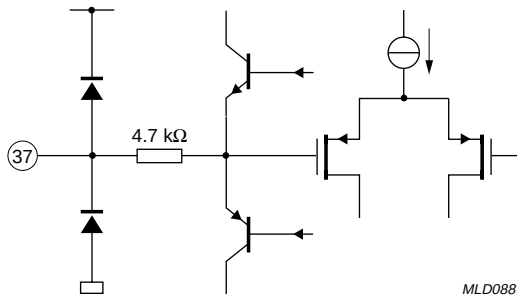
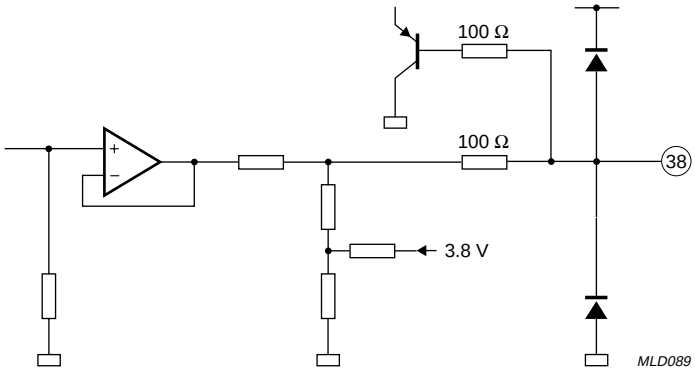
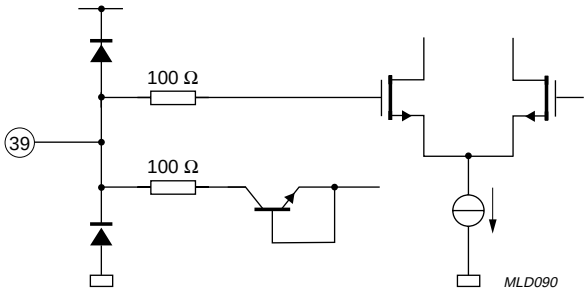
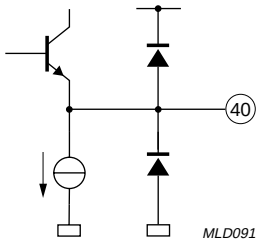
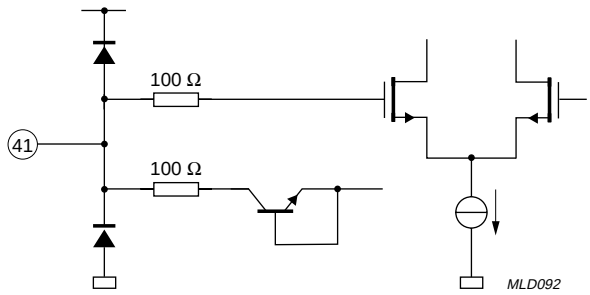
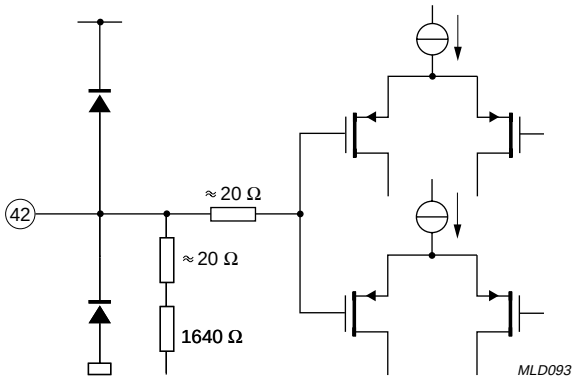
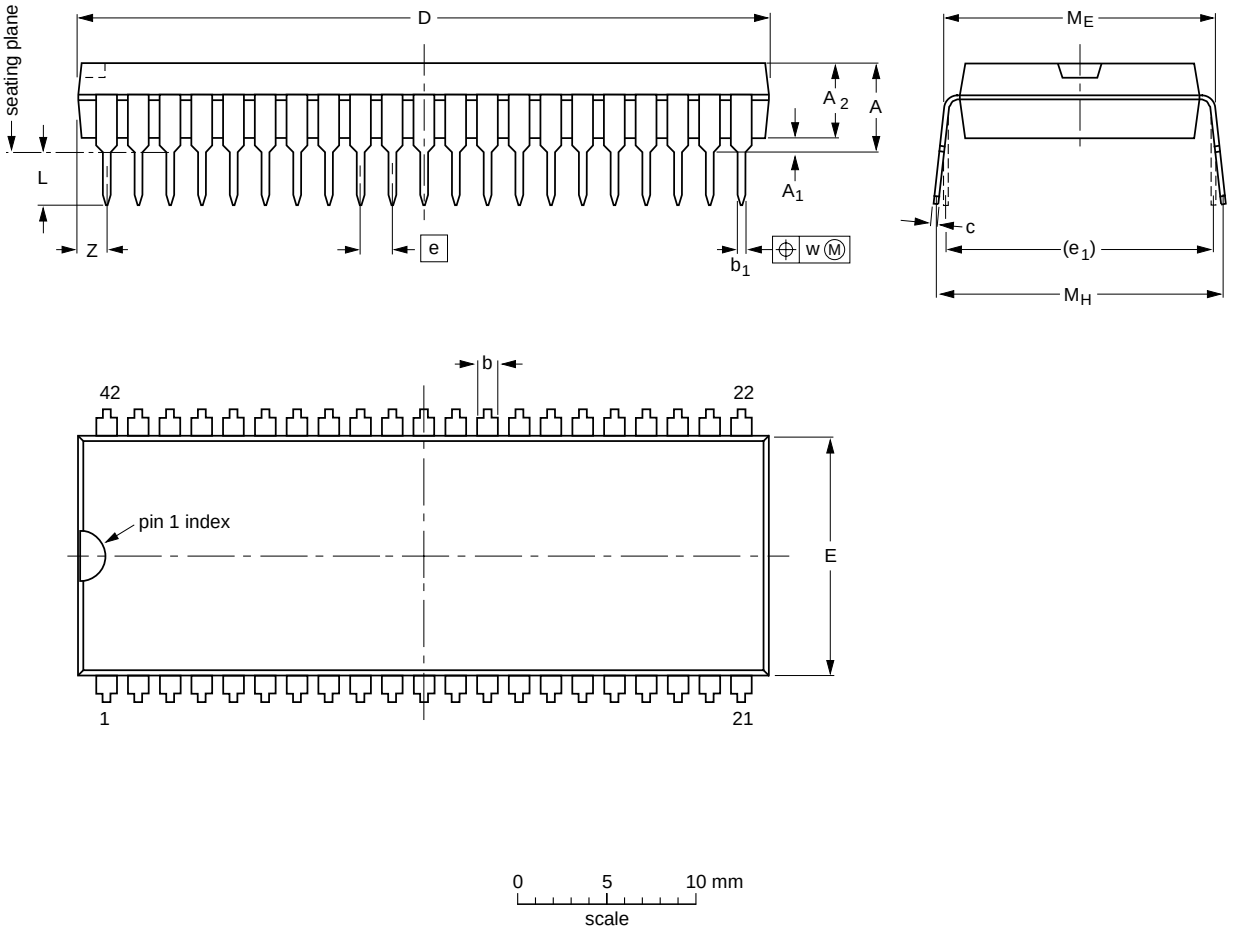
$C_{NR\ D\ L}$	36	

SYMBOL	PIN	EQUIVALENT CIRCUIT
$RECT_L$	37	
$C_{ATT/REC\ L}$	38	
PRES DET R	39	
XTAL	40	

SYMBOL	PIN	EQUIVALENT CIRCUIT
PRES DET L	41	
$C_{DC\ L}$	42	

PACKAGE OUTLINES

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

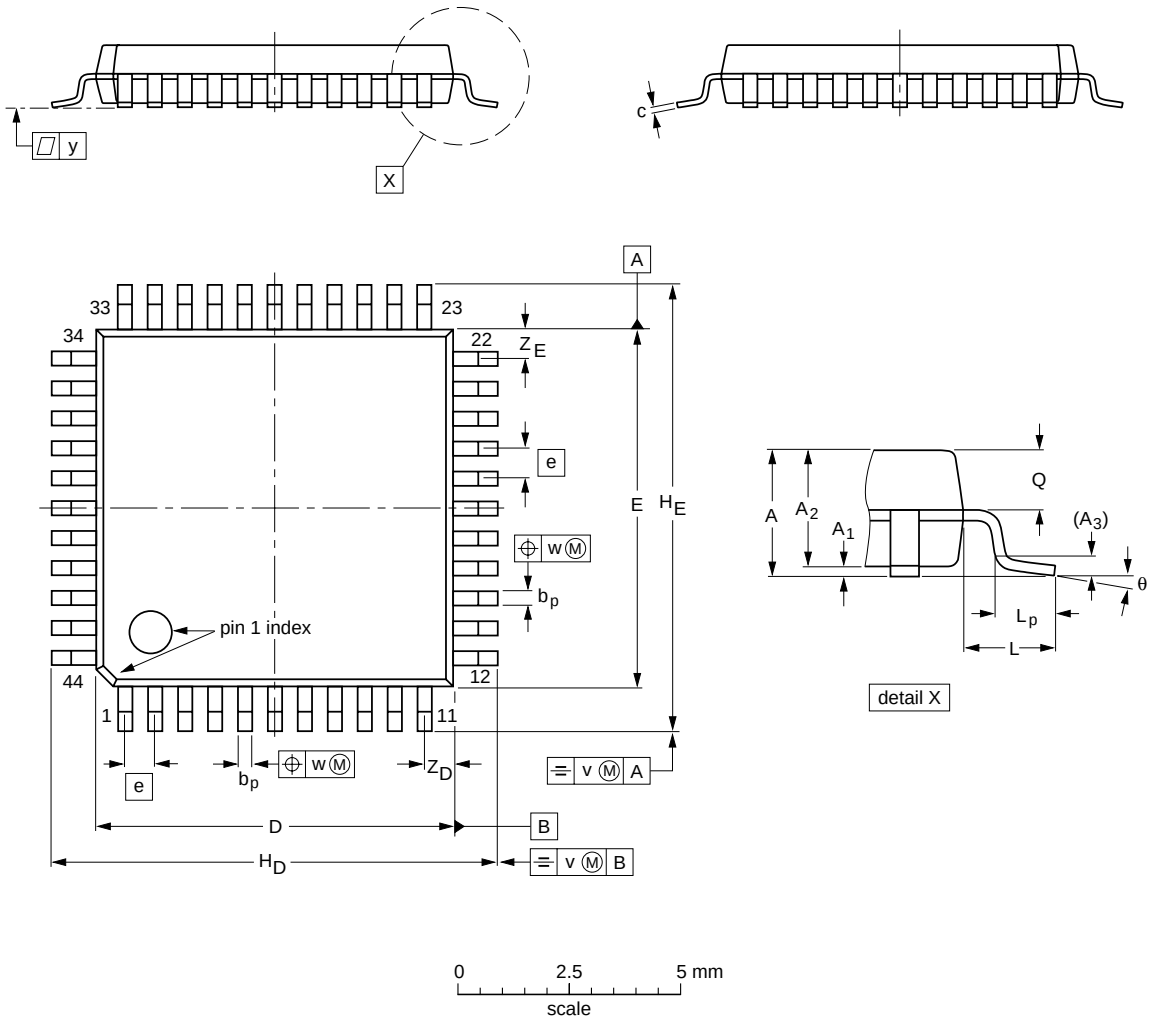
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Ukraine: Philips UKRAINE, 2A Akademika Koroleva str., Office 165,
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United Kingdom: Philips Semiconductors LTD.,
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International Marketing and Sales, Building BE-p,
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